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Modeling of Carbon Nanotube Field Effect Transistor based Amplifier in Common Source Configuration using Pspice

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***Abstract*—The carbon nanotube FET would be the revolution in the nanoelectronics and its allied areas. The conventional FET gets affected with the scalability issues. CNTFET based nanoelectronics can portray significantly remarkable performance than existing CMOS models at nanoscale dimensions. In this paper, Pspice (Personal simulation program with integrated circuit emphasis) is considered for the development of CNTFET in common source configuration with regard to small signal linear amplifiers. The equivalent circuit of cntfet is studied and implemented as subcircuit in pspice. The cntfet amplifier circuit is designed with the subcircuit and added in the library.**

***Index Terms*— CNTFET, Nanoelectronics, Pspice, Common source amplifier.**

I. INTRODUCTION

CNTFETs (Carbon Nanotube Field Effect Transistors) are the miniature devices that are explored to sustain the FET scalability while enhancing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel is made up of Carbon nanotubes (CNTs) instead of silicon. It enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon. CNTFET-based analog circuits are advantageous compared to very large scale of integration (VLSI) technologies represented by MOSFETs Ref [1].

A promising candidate which avoids these difficulties and allows further scaling down is the Carbon Nanotube Field Effect Transistor (CNTFET).CNTFET is expected for the specific behavior and electrical features. Carbon nanotubes (NT) are generally outcome of folding graphite sheets into carbon cylinders and can be termed as single (single-wall nanotube, SWNT) or several shells (multi-wall nanotube, MWNT).

II.Related work and Motivation

Carbon nanotube (CNT) shows excellent and novel performances in the field of electrical engineering. The electrical properties of CNT consist of exceptional behaviour that will help to manufacture very tiny semiconductor device Ref [2]. Modeling of the tube is studied in the recent work and in this paper, Electrical properties of CNT are addressed for the analysis of nanotube based amplifier. A tube consists of carbon

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atoms on its surface, and these carbon atoms are arranged in hexagonal patterns.
Consider a unique chiral angle for every nanotube the angle is stated by a value in the region (0, 30°). Using these definitions, the diameter of the tube can be computed using the equality of the length of the C_h and the nanotube's circumference is as follows:-

$$d_t = \frac{L}{\pi} = \frac{a}{\pi}\sqrt{n^2 + nm + m^2} \quad [1]$$

where dt is the diameter of nanotube, L is length of the chiral vector, a is basis vector and (n, m) is the chiral vector of a graphene. Depending on the folding angle and the diameter, nanotubes can assume both metallic and semiconducting behavior. Basic theory also shows that the band gap of semiconducting NTs decreases with the increasing of diameter. The MWNT's were produced by an arc-discharge evaporation technique and used without further treatments. The NT were dispersed by sonication in dichloroethane and then spread on a substrate with predefined electrodes. In figure 1 is illustrated a schematic cross section of the Intel first CNTFET device. It consists of either an individual SWNT or MWNT bridging two electrodes deposited on a 140 nm thick gate oxide film on a doped Si wafer, which is used as a back gate. The 30 nm thick Au electrodes were defined using electron beam lithography Ref[3].

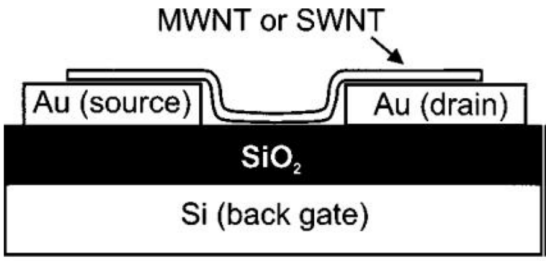

Fig.1 Schematic cross section of CNTFET

CNTFET devices can be classified in two ways: the first classification is based on the geometry of the device; the second is oriented to the type of technology used for the electrodes of the device. The classifications are discussed below:-
The main geometries for the device are related to the gate contact position:
a) Back-Gate CNTFET;
b) Top-Gate CNTFET;
c) Wrap-Around Gate CNTFET;
d) Suspended Gate CNTFET.
CNTFET-based electronic solutions could be classified for the following classes of analog circuit design application:-
a) Current and Voltage references (current mirrors, bootstrap references, etc.);
b) Operational Amplifier and OTA;
c) Waveform generator;
d) Radio Frequency application;
e) Comparators and other Mixed A/D circuits;
f) Optoelectronic and Sensing applications.

III. Problem Statement

The CNTFET technology and traditional MOSFET circuit application performances for the same circuit through PSPICE simulations require a compact model of CNTFET, easily implementable in simulation SPICE software to design analog circuits. Carbon has four valence electrons, three are used for the sp2 bonds. In sp2-hybridization, an electron is promoted from the 2s-orbital to a p-orbital, and then two electrons from different 2p-orbitals combine with the single electron left in the 2s-orbital to generate three equivalent sp2-orbitals.These orbitals are planar with 120 degree between the major lobes, and the remaining p-orbital is perpendicular to this plane .The leftover p-orbital is perpendicular to the graphene, and electrons in this orbital bond to other carbon atoms through weak pi-bonds.The electrons in the p-orbitals are thus loosely bound and responsible for the conductance of graphite. Since the CNT is made up of one or more sheets of

graphene rolled up in a tubular structure, the binding in the CNT is nearly identical to that of graphite.The miniaturization has always a vital role in electronic evolution: at each generation, the miniaturization permits to obtain good speed, lower power dissipation, lower costs and more number of gates on chip. Nowadays, the conventional devices are very smaller, and a further reduction in size would impact tunnel effects thus degrading the whole performance. Therefore, the scientific community is looking for a new kind of device, compatible at nanometer scale, which is the ultimate limit in miniaturization. The most reliable language available nowadays is SPICE, or any of its evolution, with various graphic interfaces. Another language having a solid implementation is Verilog-A, which is very interesting since it allows device description in a syntax quite near to C programming language. The electrical properties of CNT consist of exceptional behaviour that will help to design very tiny semiconductor device. Reduction of energy loss in a semiconductor device becomes more challenging task normally. Tiny size of electronics device is widely expected to everyone those who believe to have the compactness in the model. Digital devices become compact due to small size of the electronics devices. As the technology advances, the demand for scaling down has gone high. The CMOS illustrates various poor effects of scaling down. Some of them are short channel effects, carrier effects and drain induced barrier dissolving. Prediction through modeling forms the basis of engineering design. The computational power at the fingertips of the professional engineer is increasing enormously and techniques for computer simulation are changing rapidly. Engineers need models which relate to their design area and are adaptable to new design concepts. They also need efficient and friendly ways of presenting, viewing and transmitting the data associated with their models.

IV. Design- Subcircuit in Pspice

The cntfet is drawn in pspice as a subcircuit and saved for future applications .The circuit consists of source ,drain and gate as ports with capacitances and resistances. The circuit is designed and can be called for the circuit designing of cntfet amplifier in common source configuration. The figure 1 indicates the carbon nanotube FET which would result in a circuit for various applications.

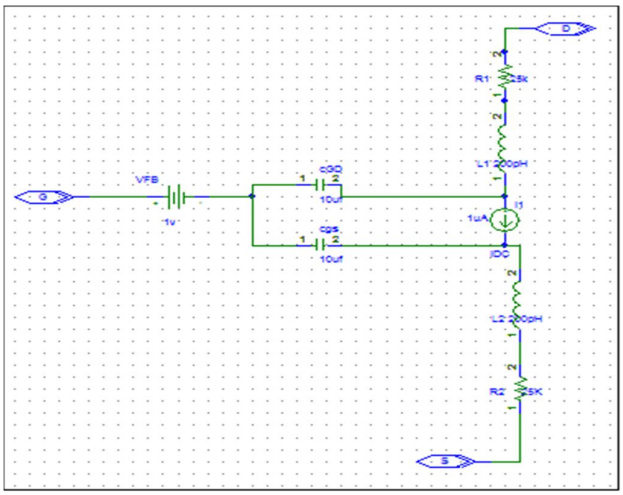

Fig.2 CNTFET equivalent circuit

Model in figure 2 involves the quantum capacitances CGD and CGS, which represent the gate to CNT capacitances.CNT quantum inductance, assumed, in the proposed model, constant and equal to 400 pH/nm, which is splitted up into two inductances of 200 pH/nm, while the classical self-inductance can be ignored. Amplifying is the application where analogue function is utilized with CNTFETs .In this case, results are expected to be consolidated as far as the power consumption is concerned.

CNTFETs have high transconductance at an acceptable low channel capacitance and offer the highest potential for gate control. The modeling of cntfet is introduced in this paper which encompasses the ease of simulation with proper selection of resistance and capacitances. The simulation underlines that CNTFETs works better than MOSFETs as shown in figure 3.It includes three resistances of 5Kohm and input source is connected to Gate, and drain via resistor to biasing voltage.

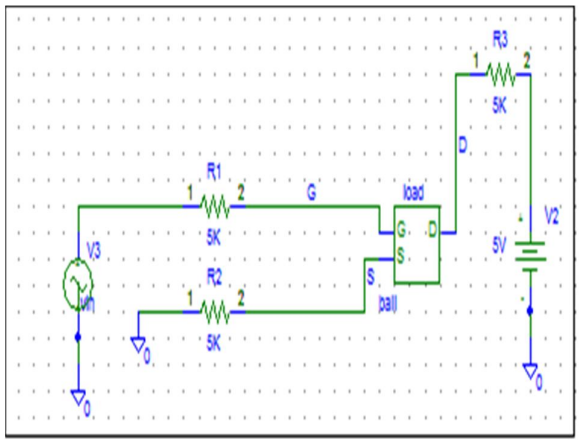

Fig.3 CNTFET as an amplifier

V. About CNTFET-Methodology

As one of the upcoming new devices, CNTFET ignores most of the limitations for traditional silicon devices.Theoretical advantages in using CNTFET-based analog circuits are studied with relevance to nanoscale devices. A model describing the common source configuration for the good amplification is depicted in this paper .The cntfet is treated as subcircuit which can be considered for big circuits Ref(3).

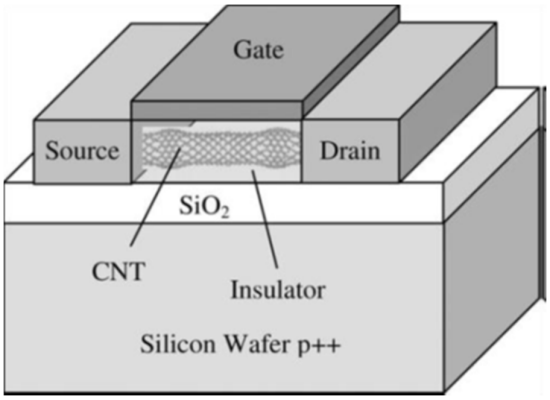

Fig.4 Representation of CNTFET

The Figure 4 depicts the 3-D image of CNT based FET.The advantages of carbon nanotube like high electrical and thermal conductivity because of their nanostructure and the strength of the bonds between carbon atoms lead to similar applications as of conventional Mosfet. A typical layout of a MOSFET-like CNFET device is as shown above where the CNT channel region is undoped, and other regions are heavily doped. This model serves as a starting point towards the complete CNFET-device model, which includes the formation of subcircuit which would be introduced in big and complicated circuits ,thereby reducing the space and complexity .Other modeling parameters are not discussed here in this paper. The subcircuit is the stepping stone for many analog circuits. The three terminals are gate ,drain , and source which have usual meanings and functions.

Figure 5 is illustrating one example of multichannels included in CNTFET application .One single walled carbon nanotube channel is capable of handling 2-3 field effect transistors.

In this example, three CNFETs are fabricated along one single CNT. The channel region of CNTs is undoped, whereas the other regions of CNTs are heavily doped Ref (4). The model presented in this article would be taken into consideration for different applications like transistor switch, variable resistor, and amplifier. The amplifier with common source configuration using cntfet would have high input impedance and low channel resistances. The conversion of gate-source voltage into a small signal drain current would lead to an amplified voltage across the load resistor Ref (5).

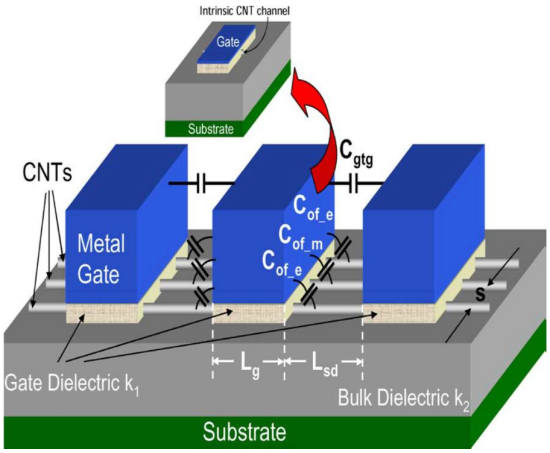

Fig.5 CNTFET with multiple channels

VI. Results and Discussions

The model described in this paper is an initiative leading to the entire CNFET device model.The additional device/circuit-level nonidealities and multiple CNTs should be the next level for other applications. The conventional Mosfet is the backbone for this type of change in the channel constructed with carbon nanotube. The pluses of carbon nanotube in nanotechnology application are studied in this paper as far as the properties are concerned. larger current carrier mobility in CNTs compared to bulk silicon has been observed .

VII. Conclusion

The Pspice circuit simulator is used to design relevant circuits as the common source cntfet amplifier.The subciruit is drawn with input and output ports with supporting capacitances and resistances .Here, in this paper,student version of Pspice is used.The model can be implemented to carry out static analysis of digital gates as well. The intrinsic drain current and terminal charges are the parameters for modeling The virtual source modeling with the virtual source velocity extracted for different channel lengths (ranging from 3-um down to 15-nm).

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